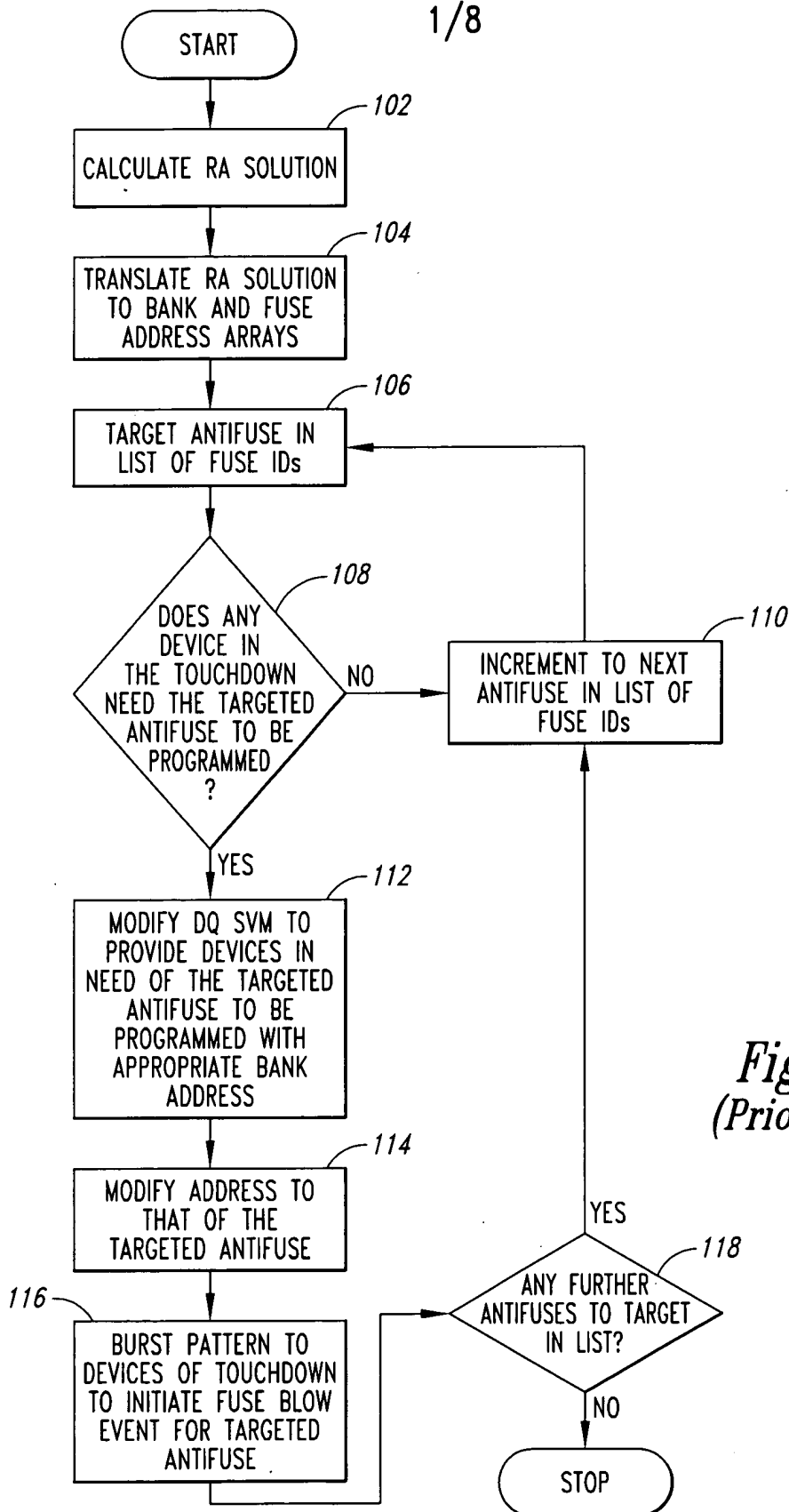




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*Fig. 1*  
*(Prior Art)*

The diagram illustrates a memory system 300. It features four memory banks: BANK0, BANK1, BANK2, and BANK3. Each bank is associated with a control logic block (340, 342, 344, 346) and a data latch (BANK LATCH0, BANK LATCH1). The control logic blocks receive control signals (CNTRL0, CNTRL1, CNTRL2, CNTRL3) and address signals (A0-AN). The data latches receive address signals (A0-AN) and output data signals (BANKLATCH0, BANKLATCH1). A central LOGIC CIRCUITY block (350) receives data signals (DQ0, DQ1, DQ2, DQ3) and control signals (CNTRL0, CNTRL1, CNTRL2, CNTRL3) and outputs control signals (BANKLATCH0, BANKLATCH1).

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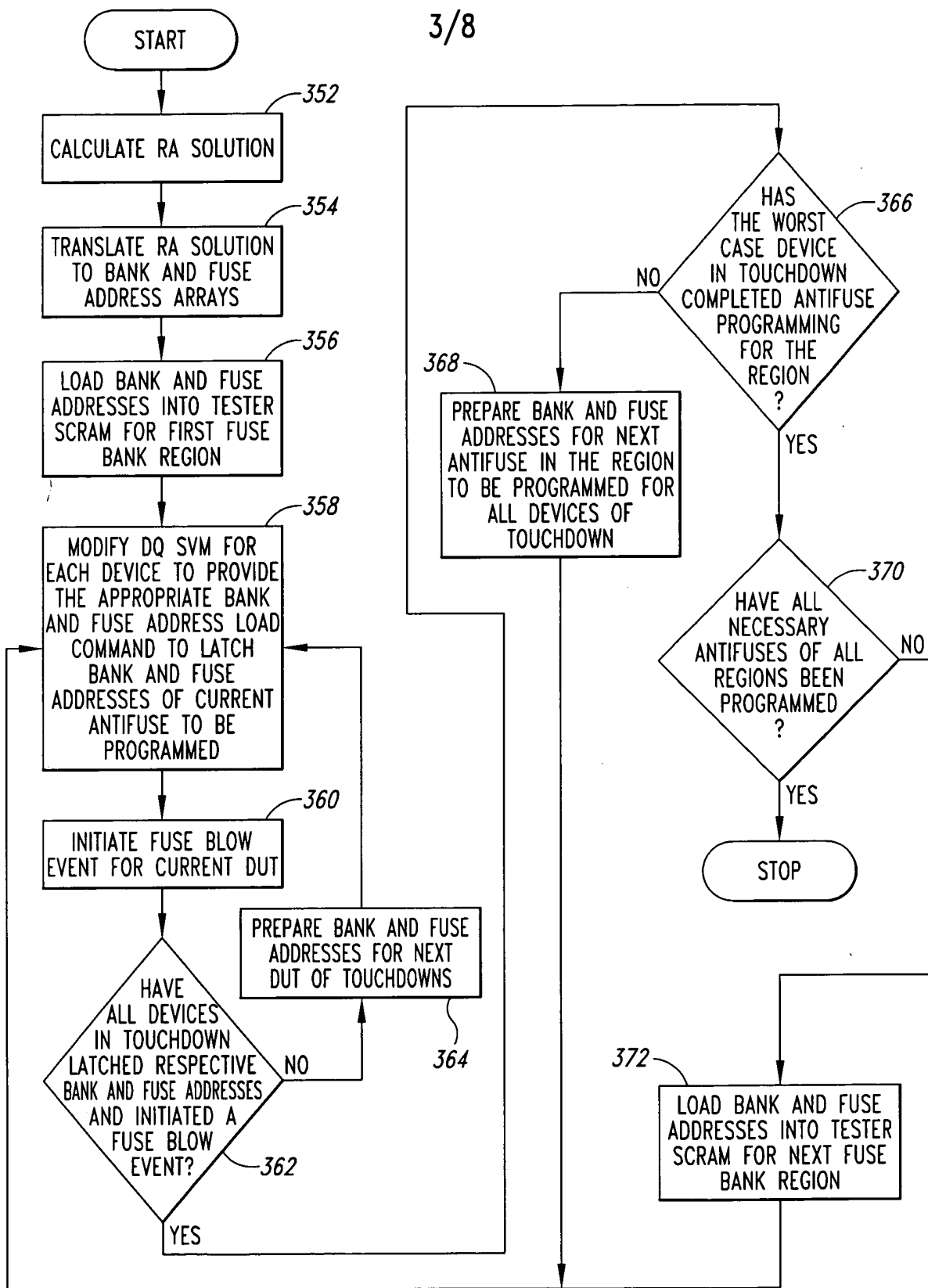


Fig. 3

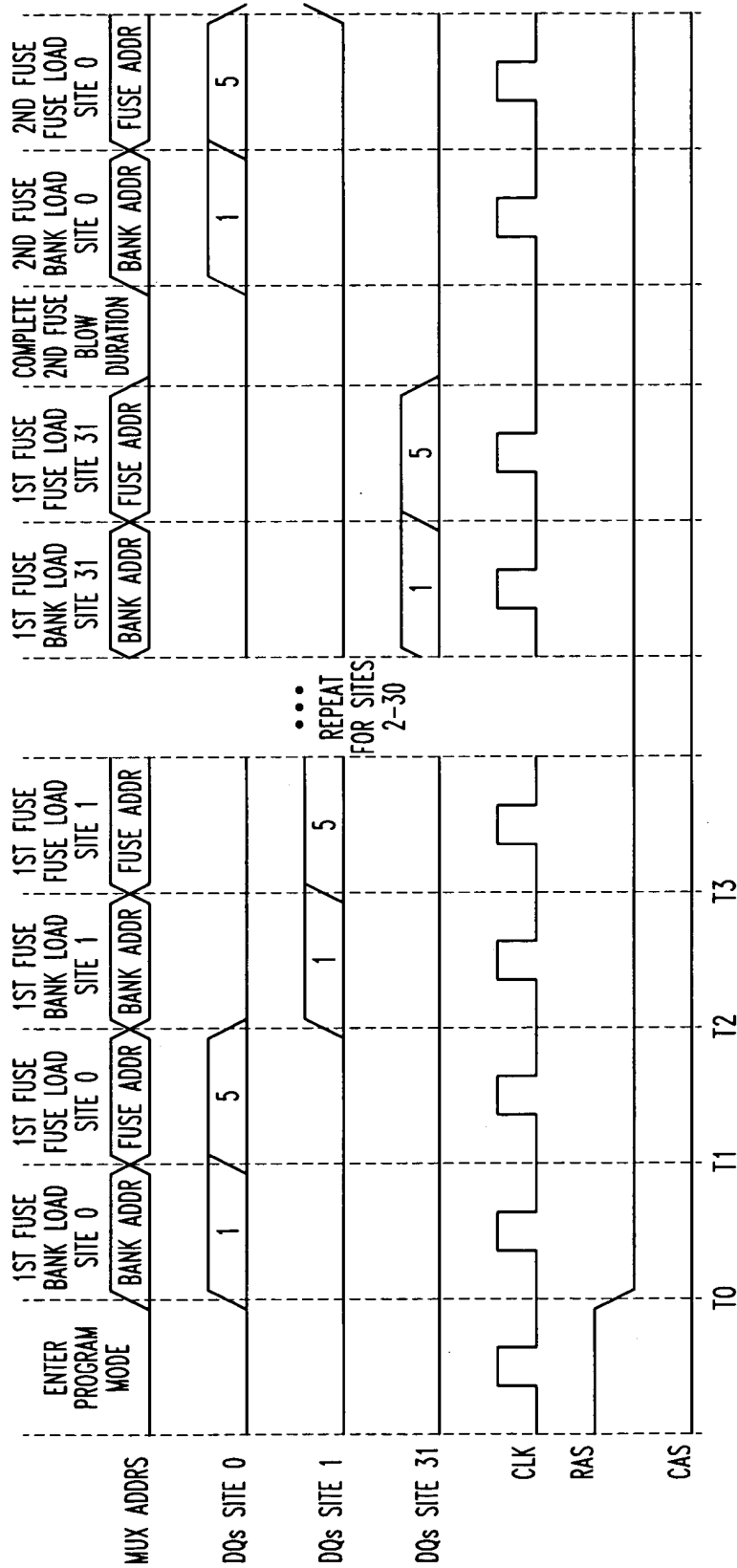


Fig. 4



500

SCRAM RAM		DQ SVM DATA			
		DUT 0	DUT 1	DUT 31	DUT 63
		0123	0123	0123	0123
502	BANK	1000	0000	0000	0000
504	FUSE	1010	0000	0000	0000
502	BANK	0000	1000	0000	0000
504	FUSE	0000	1010	0000	0000
502	BANK	0000	0000	1000	0000
504	FUSE	0000	0000	1010	0000
502	BANK	0000	0000	0000	1000
504	FUSE	0000	0000	0000	1010

Fig. 5

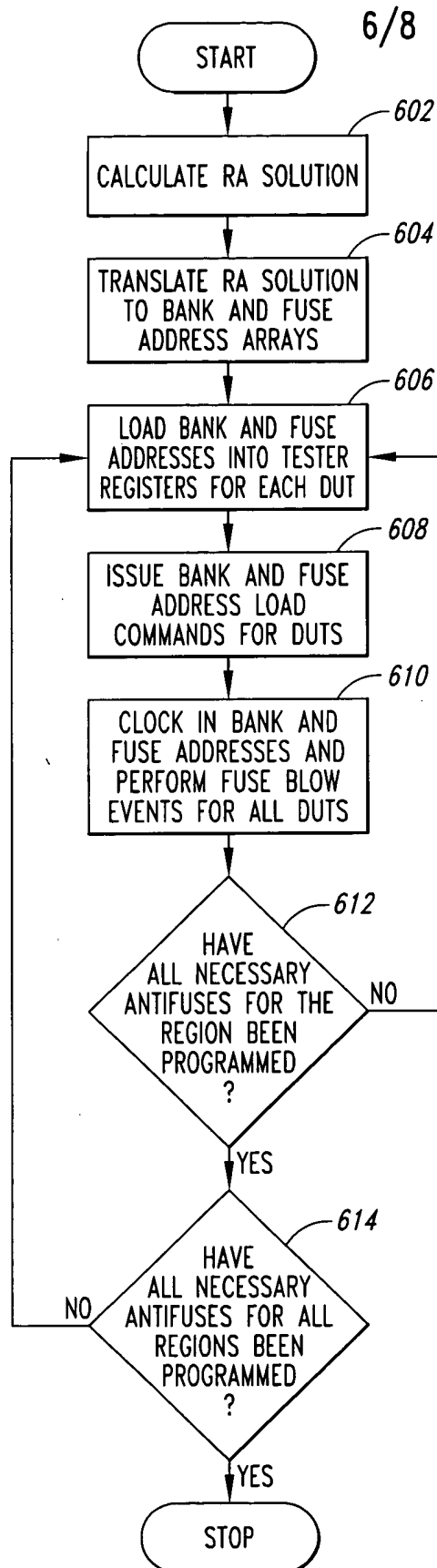


Fig. 6

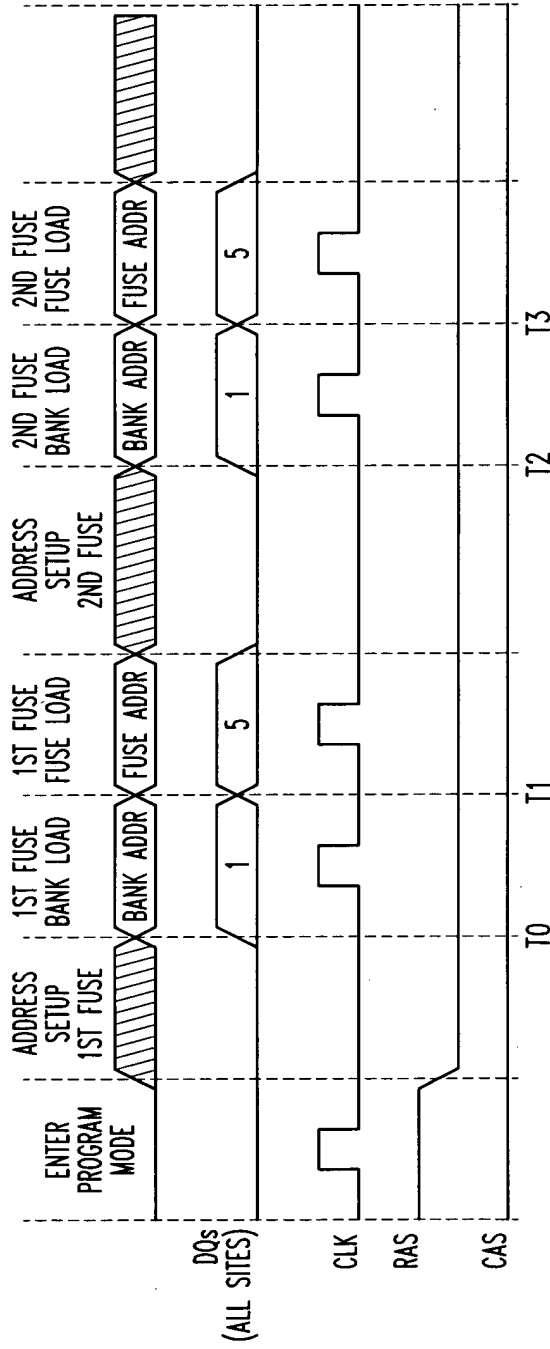
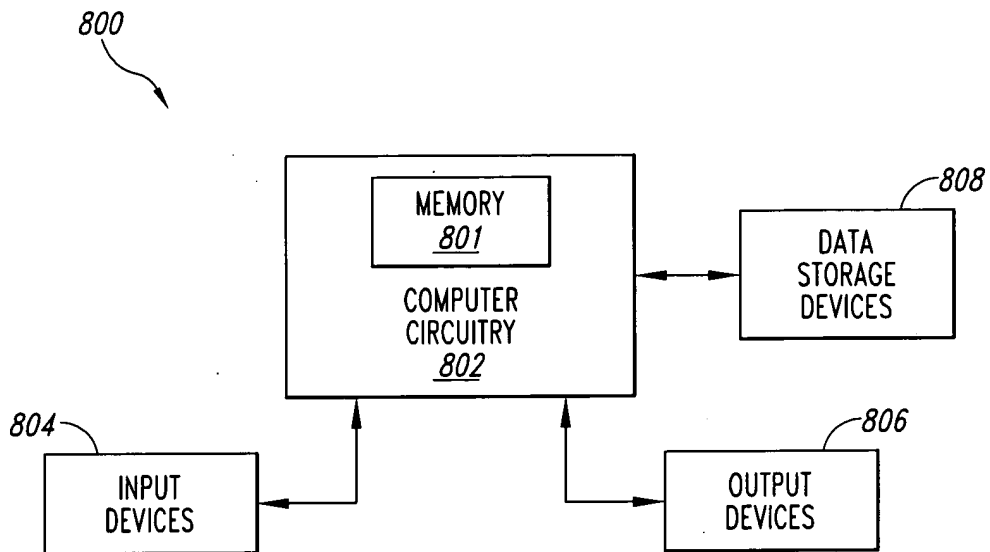


Fig. 7



*Fig. 8*